

Abstract of the Disclosure

A multiply-accumulate circuit includes a compressor tree to generate a product with a binary exponent and a mantissa in carry-save format. The product is converted into a number having a three bit exponent and a fifty-seven bit mantissa in carry-save format for accumulation. An adder circuit accumulates the converted products in carry-save format. Because the products being summed are in carry-save format, post-normalization is avoided within the adder feedback loop. The adder operates on floating point number representations having exponents with a least significant bit weight of thirty-two, and exponent comparisons within the adder exponent path are limited in size. Variable shifters are avoided in the adder mantissa path. A single mantissa shift of thirty-two bits is provided by a conditional shifter.

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